IN THE SPECIFICATION

Please amend the following paragraph, on page 13, line 6, as follows:

A manufacturing method of the vertical planar type MOSFET 1 shown in FIG. 1 will be described with reference to cross-sectional views of FIGS. 2 through 8. First, as shown in FIG. 2, the drift layer 102 of the first conductivity type is formed by epitaxial growth and the like on the semiconductor substrate W which is to be a drain layer. Then, the oxide film 10 is formed on the drift layer 102 by using a thermal oxidation technique or the like. Subsequently, the cell portion Rc and a part of the terminating portion Rt of the MOSFET are selectively etched and removed from the oxide film 10 by using a photolithography technique and the like. In this embodiment, since removal is carried out by wet type etching, an end portion of the oxide film 10 on the side of the cell portion has a tapered shape, and a gentle inclined surface remains. Subsequently, the gate oxide film 104 is formed on the surface of the drift layer 102 by using the thermal oxidation technique or the like, and polysilicon is grown on the gate oxide film 104 by using a CVD technique or the like. Then, as shown in FIG. 3, polysilicon on the gate oxide film 104 is selectively eliminated by patterning and etching using the photolithography technique and the like so as to leave an area for the gate 106 of the MOSFET and an area for the field plate electrode 20. Then, the second conductivity type impurity ions are implanted into the drift layer 102 using the polysilicon 106 and 20 as masks, and then the cell portion base layer 108 and the terminating portion base layer 40 are formed by thermodiffusion processing and the like as shown in FIG. 4. Thereafter, as shown in FIG. 5, the high-concentration impurity diffused layers 110 and 42 of the second conductivity are selectively formed in the cell portion base layer 108 and in the terminating portion base layer 40, respectively, by the photolithography technique, the impurity ion implantation, the thermodiffusion processing and others. Here, the mask of the terminating portion high-concentration impurity diffused layer 42 is formed so as to be positioned on the inner side away from the field plate electrode 20 and on the outer side area from a formation plan area of the later-described side wall spacer 16 (see FIG. 8). At this time, it is desirable to perform patterning in an inner area away from the field plate electrode 20 on the oxide film 10. Furthermore, as shown in FIG. 6, the source layer 112 is selectively formed in a surface layer of the cell portion base layer 108 by using a known technique. Then, as shown in FIG. 7, an insulating film is deposited on the surface by using the CVD technique, and the side wall spacers 114, 16 and 14 are formed by utilizing a step between the gate electrode 106 and the substrate surface by anisotropic etching. Subsequently, a high-melting point metal such as titanium (Ti) is deposited on the surface by a sputtering technique and the like, and the high-melting point metal is caused to react with the gate electrode polysilicon 106, the field plate electrode ~~22~~20 and the substrate surface silicon by a heat treatment, thereby forming the metal silicide layers 116, 118, 44 and 22. The metal which does not react with silicon is selectively removed by subsequent etching. Then, as shown in FIG. 8, an interlayer insulating film 122 which insulates the gates and the sources from each other is formed by the CVD technique or the like, this insulating film is selectively eliminated by etching utilizing the photolithograph technique, and a contact hole for the source electrode is formed. Subsequently, a metal having, e.g., aluminium (Al) as a main component is deposited by a sputtering technique and the like, this is selectively removed by etching utilizing the photolithography technique or the like, and the gate electrode 106 and the source electrode 132 are lead out to the outside (not shown). At last, a drain electrode 152 is formed on the lower side of the semiconductor substrate W. With the above-described steps, the power MOSFET 1 of the first embodiment of the semiconductor device according to the present invention can be manufactured. Since the terminating portion thus formed has the high-concentration impurity layer 42 on the outer side of the metal silicide layer 44, the high reliability can be assured even if a high breakdown voltage is used.

Please replace the Abstract on page 32, lines 1-30 with the following: